

10/8/15, 397
8/6/08
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AMENDMENTS TO THE SPECIFICATION

Please amend paragraph 0015 as follows:

[0015] Under an embodiment of the invention, a processor architecture may ~~supports~~ support control speculation by providing two instructions, the instructions being a speculative load instruction (which may, for example, be designated as ld.s) and a speculation check instruction (which may, for example, be designated as chk.s). A processor utilized in an embodiment of the invention may include an Intel Itanium or Intel Itanium 2 processor. Under an embodiment of the invention, a processor does not generate a fault if a speculative load (ld.s) causes a hardware exception, such as a misaligned access exception. Instead, the processor invalidates the result of the load by making a particular setting, such as setting the NaT (not a thing) bit representing the 65th bit of an integer register for the Intel Itanium Processor Family (IPF) architecture. The speculation-check instruction (chk.s) checks the NaT bit and branches to a recovery code if the speculative load fails, indicated by the NaT bit being set. The control speculation feature generally allows a compiler to schedule a load speculatively above program branches upon which the load is control dependent. Under an embodiment of the invention, a control speculation feature or process is further used to implement read barriers in a managed runtime environment.

Please amend paragraph 0032 as follows:

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[0015] Portions of the present invention may be provided as a computer program product, which may include a machine-readable medium having stored thereon instructions, which may be used to program a computer (or other electronic devices) to

AB
10/8/15, 397
8/6/08